UNITED STATES PATENT AND TRADEMARK OFFICE

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EXAMINER
HOYE, MICHAEL W

ART UNIT	PAPER NUMBER
2614	

DATE MAILED: 12/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

PTO-90C (Rev. 10/03)

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on _22 September 2005_.

2a)☐ This action is **FINAL**.   2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) _2-23_ is/are pending in the application.

    4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) _2-13,22 and 23_ is/are allowed.

6)☒ Claim(s) _14-21_ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on _12 February 2003_ is/are: a)☒ accepted or b)☐ objected to by the Examiner.

    Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

    Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

    a)☐ All   b)☐ Some * c)☐ None of:

      1.☐ Certified copies of the priority documents have been received.

      2.☐ Certified copies of the priority documents have been received in Application No. _____.

      3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

    * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1)☐ Notice of References Cited (PTO-892)

2)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)

3)☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
    Paper No(s)/Mail Date _____.

4)☐ Interview Summary (PTO-413)
    Paper No(s)/Mail Date. _____ .

5)☐ Notice of Informal Patent Application (PTO-152)

6)☐ Other: _____.

DETAILED ACTION

Response to Arguments

1.   Applicants' arguments originally filed on July 21, 2005 and entered with the filing of a

RCE on September 22, 2005, with respect to claims 14-21, have been fully considered but they

are not persuasive.

Regarding claims 14-17, the Applicants' argue on page 8 that, "claim [14] requires

storing at least a portion of the compressed transport stream data signals, via a first bus, and a

memory buffer controlled by the secondary set of control signals and sending the contents of the

memory buffer, via the first bus, to a system bus. Applicants respectfully submit that such an

operation or structure is not taught or suggested by the Cheney reference alone or in combination

with the So reference."

The Applicants' further argue on pages 8-9 and more specifically on page 9 that, "The

control signals generated, apparently by the frame buffer pointer control 686 actually appear to

control based on the type of display mode that has been selected via the display mode switch

logic 696 and not from the compressed transport stream control signals as noted in the claim."

In response, the Examiner respectfully disagrees with the Applicants regarding the

complete characterization of the Cheney reference as described above. While Cheney does

disclose that the frame buffer pointer control 686 may produce control signals based on the type

of display mode that has been selected, the frame buffer pointer control 686 produces control

signals based on the B picture "MPEG-2 repeat field" and VSYNCH signals it receives as well

(see cols. 11-12 of Cheney and a complete description in the rejection of claim 14 below). Also,

while it was previously noted by the Examiner that while the Cheney reference discloses a PCI

bus 42 (Fig. 2), the Cheney reference does not explicitly disclose the claimed sending the

contents of the memory buffer via the first bus to a system bus. The So reference was provided

as evidence and motivation for the claimed structure as described in the claim.

Regarding claims 18-20, the Applicants argue on page 9 that, "As to claim 20, the final

action did not appear to address Applicants' previous remarks. Applicants respectfully reassert

the relevant remarks made in the previous office action..."

In response to the Applicants arguments or comments above, which appear to be referring

to all of claims 18-20, the Examiner respectfully notes that in the non-final office action which

preceded the final office action referred to above, claims 18-20 were rejected under 35 U.S.C. §

102(e) as being anticipated by Schindler (USPN 5,900,867), and were also rejected alternatively

under 35 U.S.C. § 103(a) as being unpatentable by Schindler (USPN 5,900,867). In the

following office action, the final rejection mailed on May 18, 2005, amended claims 18-19, and

claim 20 were rejected in a new grounds of rejection under 35 U.S.C. § 103(a) as being

unpatentable by Schindler (USPN 5,900,867), in view of So (USPN 5,909,559). The Examiner

is uncertain of what relevant remarks were not addressed and respectfully requests the

Applicants to reiterate any relevant arguments related to the new grounds of rejection presented

in the previous final office action and presented again in this office action in any future

correspondence with the Patent Office.

Regarding independent claim 21, the Applicants' argue on page 9 that, "The claim requires that the same frame buffer store, for example, one line of frame buffer memory as pixel information of a video image to be displayed wherein in a second mode of operation compressed transport stream data is stored in the frame buffer wherein one line of the frame buffer memory is representative of one transport stream packet. Such a method does not appear to be taught by the combination of the references since it appears that the references do not include the teachings alleged in the Office Action and do not appear to provide any motivation for their combination."

In response to the Applicants' argument that the same frame buffer store the video data for both modes of operation. The Examiner refers the Applicants to col. 11, lines 34-52 (specifically lines 49-52) of the Schindler reference, where the MPEG data (compressed video) may be provided back to controller 510, which then places the video information into dynamic random access memory (DRAM) or video random access memory (VRAM) **518**. The **VRAM 518** is a frame buffer which buffers the video before it is transmitted for display. Moreover, the Schindler reference primarily discloses high-level system components, whereas, the Malladi and Datari references where provided to give additional teaching related to the specifics of frame buffer memory storage methods, which one of ordinary skill in the art of frame buffer memory use would look to in order to arrive at the Applicants claimed invention. More specifically, the Malladi reference explicitly states in col. 4, lines 35-37 that, "Storing pixel data in pages on a scan line basis is **optimum** for pictures or frames which are to be displayed." Therefore, the Malladi reference provides motivation for the claimed, "storing pixel information in a frame buffer of a video adapter, wherein one line of the frame buffer memory is representative of one line of a video image to be displayed." In addition to, the Datari reference teaches that MPEG

video data packets may be stored or buffered in memory and sequentially accessed by **priority** (see col. 5, lines 13-42 and col. 6, lines 62-66, also see col. 8, lines 10-18). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to have further combined the method of Schindler et al which discloses multiple modes of operation and storing video data, with the Datari reference, which specifically teaches that a line of the frame buffer memory may be representative of one MPEG or transport stream packet for the advantage of providing a storage format which allows for **improved priority accessing** of transport stream packets of video images to be displayed.

The Applicants also argue on page 10 that, "Schindler does not describe a video graphics adapter as claimed, but to the contrary, a video graphics adapter card wherein the compressed video is stored in the frame buffer memory."

In response to Applicants' argument that the references fail to show certain features of Applicants' invention, it is noted that the features upon which applicant relies (i.e., a video graphics adapter) are not recited in the rejected claim. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*. 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993). Claim 21 currently states in part, "A method of storing video data..." and "...storing pixel information in a frame buffer of a video adapter..." According to the broadest reasonable interpretation of the claim there seems to be no distinction between the claimed, "frame buffer of a video adapter", and a "frame buffer of a video graphics adapter card", as disclosed in the Schindler reference. If the Applicants' intend the claimed "video adapter" to be only a single chip, then feature should be recited in the claim.

Finally, the Applicants argue that, "Schindler does not describe, as admitted by the Office

Action, the storing of compressed video..."

In response, the Examiner respectfully disagrees with the Applicants characterization of

the Office Action. The Examiner did describe anywhere in the Office Action that Schindler does

not describe the storing of the compressed video, but to the contrary, Schindler does describe

receiving and storing compressed or MPEG video data in DRAM or VRAM 518 (see col. 11,

line 34 – col. 12, line 3).

Claim Objections

2.   Claim 18 is objected to because of the following informalities: in lines 7-10, the claimed,

"...and further includes a graphics engine operative to decompress the compressed transport

stream, a graphics engine and a video output port", seems to be repeating the "graphics engine"

twice and should be reworded as --**and further includes a graphics engine operative to**

decompress the compressed transport stream, and a video output port--. Appropriate

correction is required.

Claim Rejections - 35 USC § 103

3.   The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all

obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in
> section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are
> such that the subject matter as a whole would have been obvious at the time the invention was made to a person
> having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the
> manner in which the invention was made.

4.   Claims 14-17 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cheney et

al (USPN 6,519,283), in view of So (USPN 5,909,559), both cited by the Examiner.

As to claim 14, note the Cheney et al reference which discloses a method of receiving

video graphics data. The claimed "receiving a compressed transport stream associated with a

digital video broadcast signal" is met by the digital video from cable or satellite broadcast signal

101 (Fig. 4) received at NIM 102, where a MPEG transport stream is sent to transport logic

(XPORT) 103 (see col. 6, line 35-45). The MPEG transport stream is a compressed transport

stream. In addition, the claimed "compressed transport stream having data signals and control

signals" is inherent to a MPEG transport stream. The Applicants also disclose this in the

"Background of the Invention" (or prior art) section of the specification, which describes the

Digital Video Broadcast (DVB) transmission standards and specifically states that, "The

compressed MPEG 2 format is referred to as a transport stream. The transport stream from the

demodulator comprises a plurality of packets. Each of the transport stream packets comprises

one synchronization byte, followed by one of 187 data bytes or 187 data bytes plus 16 extra

bytes depending on the format." (See Specification, page 1, lines 15-19), in addition to, it is well

known in the art that MPEG transport streams may comprise header information with routing

information. Therefore, it is well known in the art that a MPEG transport stream comprises data

signals as met by the data byes, and control signals as met by the synchronization bytes and

header information. The claimed "generating a secondary set of control signals from the

compressed transport stream's control signals" is met by the video decode system of Figure 6,

where the MPEG input source is fed through the memory control unit 652 as coded MPEG 2

video data to the input of video decoder 654 and from the Huffman decoder 672 a B picture

"MPEG-2 repeat field" signal is sent to display mode switch logic 696 (which also receives a

vertical synchronization (VSYNC) signal that is an external synchronization signal) and frame

buffer pointer control 686, and from the decoded signals from the MPEG transport stream's

control signals, along with other signals, the frame buffer pointer control 686 generates

additional control signals (see col. 9, line 31 – col. 12, line 63). More specifically, as described

above, a B picture "MPEG-2 repeat field" signal from Huffman decoder 672 of video decoder

654 may be used in part by frame buffer pointer control 686 in Fig. 6 (col. 11, line 5 – col. 12,

line 63). The claimed "storing at least a portion of the compressed transport stream data signals

via a first bus in a memory buffer controlled by the secondary set of control signals" is met in-

part by the frame buffer pointer control 686, in one mode, controlling the rotation of the frame

buffers as described above (also see col. 10, lines 37-41 and col. 11, line 5 – col. 12, line 63).

Although the Cheney reference discloses a PCI bus 42 (Fig. 2), the Cheney reference does not

explicitly disclose the claimed sending the contents of the memory buffer via the first bus to a

system bus. The So reference discloses improved integrated circuits and computer system

embodiments for desktop and computers, television sets, set-top boxes and appliances improved

with asymmetrical multiprocessors (see col. 129, lines 22-37). More specifically, the So

reference teaches the use of a multimedia system with multiple buses, including a PCI bus or bus

124 in Fig. 1 (330 in later Figs.), as well as the claimed, "sending the contents of the memory

buffer via a first bus to a system bus" as met by the embedded frame buffer 128 sending the

contents of the memory buffer via the AGP bus to the AGP port of the north bridge chip 108,

where the contents may be sent to the PCI or system bus 124/330 through the PCI port (see Figs.

1 and 126-127 and col. 129, line 23 – col. 131, line 30). Therefore, it would have been obvious

to one of ordinary skill in the art at the time of the invention to have combined the method of

receiving video graphics data as disclosed by the Cheney et al reference with the teachings the

So reference which discloses using a north bridge integrated interface for multiple buses in

conjunction with the frame buffer memory and a system or PCI bus for the advantage of having

the ability to receive various types of broadcasts or multimedia streams through a computer

system with a video graphics adapter or graphics engine and bus type system. One of ordinary

skill in the art would have been led to make such a modification since television/multimedia

receivers used with computers are well known in the art to provide additional capabilities within

a computer system.

As to claim 15, the Cheney reference discloses multiple modes of operation and a method

of receiving a digital video signal that is of a different type than the compressed transport stream,

which is met by the video signals received at 104 in Fig. 4 (col. 4, lines 40-42 & 54-57 and col.

6. lines 62-67). The Cheney reference discloses a first mode of operation as shown by receiving

a digital video signal 101, which includes a compressed MPEG transport stream (col. 6, lines 37-

44). The Cheney reference also discloses another mode of operation wherein the digital video

signal is of a different type than the compressed transport stream, which is met by the

uncompressed digital video signals received at 104 in Fig. 4 (col. 4, lines 40-42 & 54-57 and col.

6, lines 62-67), which includes data signals including pixel data signals and control signals which

are met by the corresponding synchronization signals (col. 4, lines 56-57), and by "pixel select

control" signals (col. 7, lines 40-41). The digital multi-standard decoder (DMSD) 105 provides

synchronization signals, such as, horizontal sync and vertical sync and the DMSD 105 provides

the synchronization signals to the video decoder 106 which interprets the synchronization

information and processes the data (col. 7, lines 7-18) to provide a secondary set of control

signals through the use of the frame buffer pointer control 686 and other circuitry as shown in

the video decode system of Fig. 6 and as previously described above in claim 14.

As to claim 16, the Cheney reference as combined above, further discloses a camcorder

or television camera may be used as an uncompressed signal and connected video cameras may

inherently comprise the transmission of a zoom video signal (see col. 8, lines 24-25 and ZV port

definition from the Microsoft Computer Dictionary, p. 586).

As to claim 17, the Cheney et al reference also discloses a method wherein the memory

buffer is a frame buffer as shown in Fig. 2, DRAM 53 (col. 5, lines 65-67) and Fig. 6, element

653.

5.   Claims 18-20 are also rejected under 35 U.S.C. 103(a) as being unpatentable over

Schindler et al (USPN 5,900,867), in view of So (USPN 5,909,559), both cited by the Examiner.

As to claim 18, the Schindler et al reference discloses a system for receiving a digital

video broadcast signal. The claimed "tuner to receive a digital broadcast signal and to provide

an analog output signal" is met by tuner 410 in Fig. 4, which receives a digital signal (MPEG or

MPEG-2) that is transmitted on an analog carrier signal (see col. 10, lines 31-40). The claimed

"demodulator coupled to…the tuner, and to provide a transport stream" is met by digital

demodulator 412, which demodulates the tuned signal and provides the compressed digital

MPEG transport stream signals (col. 10, lines 37-44 and 51-56). The claimed "video graphics

adapter…" is met in part by the video graphics adapter (VGA) 318, as shown in Fig. 5, where the

controller 510 or tuner 526 and/or decoder 530 send the MPEG encoded video stream to the

MPEG-2 decoder 512 (col. 11, line 34 – col. 12, line 18). The claimed "video graphics adapter

further includes a bus interface port coupleable to a central processing unit" is met by the PCI

bus interface port from controller 510 in VGA card 318 (see Fig. 5 and col. 11, lines 35-38),

which is coupleable to processor 310 via the PCI Bus (see Fig. 3 and col. 9, lines 17-24). The

claimed VGA further includes an engine, or graphics engine, operative to decompress the

compressed transport stream is met by the MPEG-2 decoder 512 in Fig. 5, which decompresses

the MPEG transport stream (see col. 11, lines 37-44), and the claimed video output port is met by

either the audio video output connector 542 (see col. 11, lines 61-63 and col. 12, lines 3-6), or

the video output 522 as shown in Fig. 5 (see col. 11, lines 40-55, more specifically lines 52-55).

The Schindler et al reference teaches that the digital video broadcast signal as described above is

transmitted through the PCI bus 312. Schindler also teaches that the VGA 318 as shown in Fig.

5 may also directly receive broadcast signals through audio and video inputs 524, 544, 546 and

548 (col. 11, lines 56-66), more specifically, standard cable connector 524, which may receive

broadcasts, is coupled to tuner circuit 526 (col. 11, lines 56-60). Although the Schindler et al

reference does not explicitly disclose that the video broadcast received through connector 524 is

a digital video broadcast, and more specifically the claimed, "transport stream port to receive the

compressed transport stream and another transport stream", the So reference teaches improved

integrated circuits and computer system embodiments for desktop and computers, television sets,

set-top boxes and appliances improved with asymmetrical multiprocessors (see col. 129, lines

22-37). More specifically, the So reference teaches the use of a multimedia system with multiple

buses, including a PCI bus or bus 124 in Fig. 1 (330 in later Figs.), as well as the claimed,

"transport stream port to receive the compressed transport stream and another transport stream"

as met by the north bridge chip 108, which has multiple ports and a PCI or system bus

connection through the PCI port to the PCI/system bus 124/330 (see Figs. 1 and 126-127 and col.

129, line 23 – col. 131, line 30). Multiple transport streams may be received through the 1394

port and/or TV tuner 130. Therefore, it would have been obvious to one of ordinary skill in the

art at the time of the invention to have combined the method of receiving video graphics data as

disclosed by the Cheney et al reference with the teachings the So reference which discloses using

a north bridge integrated interface for multiple buses in conjunction with the frame buffer

memory and a system or PCI bus for the advantage of having the ability to receive various types

of broadcasts or multimedia streams through a computer system with a video graphics adapter or

graphics engine and bus type system, in addition to providing the advantages of reducing

hardware components, simplifying the system and bypassing the PCI bus, which would cut

manufacturing costs and improve processing speed as shown by the So reference. One of

ordinary skill in the art would have been led to make such a modification since

television/multimedia receivers used with computers are well known in the art to provide

additional capabilities within a computer system and combining the components in to a single

system before connecting to the PCI bus as shown by the So reference would provide a more

efficient system.

As to claim 19, the Schindler reference discloses a memory to store at least a portion of

the compressed transport stream as met by DRAM 514 in Fig. 5 (see col. 11, lines 37-47). The

So reference as combined above with Schindler further teaches an internal memory 128 coupled

to the graphics engine 126, the transport stream port (116 of DSP1), and the system bus interface

port (PCI 122) to store at least a portion of the transport stream... as previously described above

in claim 14.

As to claim 20, the Schindler reference discloses the claimed central processor unit

coupled to the bus interface port of the video graphics adapter as met by processor 310 (see Fig.

3 and col. 9, lines 17-24), which is coupled to the bus interface port (controller 510) of the VGA

318 via the PCI BUS 312 (see Fig. 5 and col. 11, lines 35-38). The claimed transport

demultiplexer coupled to the demodulator is met by the demultiplexer 416, which is coupled to

the demodulator 412 through the F.E.C. 414 as shown in Fig. 4 (see col. 10, lines 40-58).

6.   Claim 21 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schindler et al

(USPN 5,900,867), in view of Malladi et al (USPN 5,912,676), and in further view of Datari

(USPN 6,418,169), all cited by the Examiner.

As to claim 21. note the Schindler et al reference which discloses a method of storing

video data. Schindler et al discloses multiple modes of operation, such as receiving a digital

video broadcast signal (MPEG/compressed) from a satellite dish as shown in Fig. 4, or receiving

a standard cable broadcast signal at 524 as shown in Fig. 5. The claimed first mode of operation

comprising storing pixel information in a frame buffer of a video adapter, wherein one line of

frame buffer memory is representative of one line of a video image to be displayed is met in part

by receiving an uncompressed signal from a cable video source through connector 524 (Fig. 5),

as described above, where the video signal may be buffered in VRAM 518 for output to a

monitor (see col. 11, line 34 – col. 12, line 3). Although, Schindler does not explicitly disclose

that one line of the frame buffer memory is representative of a line of video image to be

displayed, it is well known in the art of uncompressed video frame buffers that a line of frame

buffer memory may be *representative* of a line of a video image to be displayed. The Malladi et

al reference teaches that various frame storage formats exist for storing frame data in memory,

and that one method for storing a frame of pixel data is on a scan line basis, where the data is

stored in memory scan line by scan line for pictures or frames that are to be displayed (see col. 4,

lines 30-37). Therefore, it would have been obvious to one of ordinary skill in the art at the time

the invention was made to have combined the method of the Schindler et al reference which

discloses multiple modes of operation and storing video data, with the Malladi et al reference,

which specifically teaches that one line of frame buffer memory may be representative of one

line of a video image to be displayed for the advantage of providing a storage format which

provides improved or optimum performance for storing a reference frame of pixel data on a scan

line basis. The claimed second mode of operation comprising storing compressed transport

stream data in the frame buffer, wherein one line of frame buffer memory is representative of

one transport stream packet is met in part by the Schindler et al reference, which also discloses

receiving an MPEG transport stream from a digital video source Fig 4, as described above,

where the compressed MPEG transport stream is sent to the PCI bus 312, where the video

graphics adapter card receives the MPEG stream through controller 510 (Fig. 5, col. 11, lines 34-

37), and the MPEG data is routed to MPEG-2 decoder 512 with associated random access

memory (DRAM 514), which is used as buffer in assisting with the decoding (see col. 11, lines

37-47) and in lines 34-52 (specifically lines 49-52), the MPEG data (compressed video) may be

provided back to controller 510, which then places the video information into dynamic random

access memory (DRAM) or video random access memory (VRAM) **518** as used by the other

video signal described above. The **VRAM 518** is a frame buffer which buffers the video before

it is transmitted for display. Although, the Schindler et al reference does not explicitly disclose

that one line of the frame buffer memory is representative of one transport stream packet, it is

well known in the art of video transport streams that are stored in frame buffers that a MPEG-2

transport stream packet has a fixed 188 byte length as defined by MPEG standards, and

therefore, a line of frame buffer memory is *representative* of a transport stream packet since

every MPEG-2 transport stream packet has already been produced and transmitted according to

the established MPEG standards so that when received by a frame buffer memory a line of

memory is representative of one transport stream packet. In addition to, the Datari reference

teaches that MPEG video data packets may be stored or buffered in memory and sequentially

accessed by priority (see col. 5, lines 13-42 and col. 6, lines 62-66, also see col. 8, lines 10-18).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention

was made to have further combined the method of Schindler et al which discloses multiple

modes of operation and storing video data, with the Datari reference, which specifically teaches

that a line of the frame buffer memory may be representative of one MPEG or transport stream

packet for the advantage of providing a storage format which allows for improved priority

accessing of transport stream packets of video images to be displayed.

Allowable Subject Matter

7.   Claims 2-13 and 22-23 are allowed.

The following is a statement of reasons for the indication of allowable subject matter:

As to claim 22, the prior art, alone or in combination, does not teach or fairly suggest a video graphics system comprising a data storage controller having at least one pair of a plurality of internal control ports to communicate control signals within the data storage controller.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Michael W. Hoye whose telephone number is **571-272-7346**. The examiner can normally be reached on Monday to Friday from 8:30 AM to 5 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Miller, can be reached at **571-272-7353**.

Any response to this action should be mailed to:

Please address mail to be delivered by the United States Postal Service (USPS) as follows:

> Mail Stop _____
> Commissioner for Patents
> P.O. Box 1450
> Alexandria, VA 22313-1450

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Any inquiry of a general nature or relating to the status of this application or proceeding

should be directed to customer service whose telephone number is **571-272-2600.**

Information regarding the status of an application may be obtained from the Patent

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Michael W. Hoye
December 9, 2005

JOHN MILLER
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600